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EXAMINER	
TECKLU, ISAAC TUKU	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,741	MUTHUKUMAR, KALYAN	
	Examiner	Art Unit	
	Isaac T. Tecklu	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on 09/29/2003.

2. Claims 1-32 have been examined.

Oath/Declaration

3. The office acknowledges receipt of a properly signed oath/declaration filed on 09/29/2003.

Drawings

4. The informal drawings are not of sufficient quality to permit examination. Accordingly, replacement drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to this Office action. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

Applicant is given a TWO MONTH time period to submit new drawings in compliance with 37 CFR 1.81. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a). Failure to timely submit replacement drawing sheets will result in ABANDONMENT of the application.

Claim Objections

5. Claim 27 is objected to because of the following informalities: "An article" should be changed to "The article" to refer the article of claim 26. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2, 3, 21-25 and 30-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation "the group " in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 3 recites the limitation "the number of simultaneous live values" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 21 recites the limitation "the rotating stack memory locations", "the non-rotating registers" in line 6, in line 9 respectively. There is insufficient antecedent basis for this limitation in the claim.

Claims 22-25 are rejected for dependency upon rejected base claim 21.

Claim 30 recites the limitation "the rotating stack memory locations" in line 12. There is insufficient antecedent basis for this limitation in the claim.

Claims 31-32 are rejected for dependency upon rejected base claim 30.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 1-25 are rejected under 35 U.S.C 101 because the claimed invention is directed to non-statutory matter.

> The Federal Circuit has recently applied the practical application test in determining whether the claimed subject matter is statutory under 35 U.S.C. § 101. The practical application test requires that a " useful, concrete, and tangible result" be accomplished. An "abstract idea" when practically applied is eligible for a patent. As a consequence, an invention, which is eligible for patenting under 35 U.S.C. § 101, is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The test for practical application is thus to determine whether the claimed invention produces a "useful, concrete and tangible result".

Specifically, claims 1, 4, 7, 10, 14, 18 and 21 recite a method comprising spilling and filling computed values, in a register to hold addresses of spilled and filled memory locations, that are live across multiple stages in a software-pipeline loop, using rotating stack memory locations. As a whole, the claim lacks teaching as to what is being transformed or what action is taken as a result of the spilling and filling computed values. That is, comprising solely of steps of spilling and filling computed values in a register, the claim does not enable the realization of a concrete result because what result being inferred from said spilling and filling remains a concept or a non-tangible representation that cannot materialize itself out and into a tangible outcome without teaching from the claim for conveying that an explicit action is executed to yield a result based upon such said spilling and filling steps. Absent any tangible result, the claimed invention thus fails to fulfill the Practical Test Application; and is rejected for leading to a non-statutory subject matter.

Claims 2-3, 5-6, 8-9, 11-13, 15-16 and 22-25 are rejected for failing to cure the deficiencies of the above rejected non-statutory claims 1, 4, 7, 10, 14 and 25 above.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Srinivasan (U.S. 6,651,247 B1).

Per claim 1, Srinivasan discloses a method comprising spilling (col. 3, lines 50-55 "... spill one or more registers ...") and filling computed values, in a register to hold addresses of spilled and filled memory locations (col. 17, lines 21-25 "... the value stored in a memory location, the address ..."), that are live across multiple stages in a software-pipelined loop (col. 2, lines 30-40 "... fill pipeline ..."), using rotating stack memory locations (e.g. FIGURE 7C, element 7C-2 and related text).

Per claim 2, Srinivasan discloses the method of claim 1, wherein the register to hold the addresses of the spilled and filled memory locations (e.g. FIGURE 5, element 530 and related text) is selected from the group consisting of a rotating register and a non-rotating register (e.g. FIGURE 5, element 552 and related text).

Per claim 3, Srinivasan discloses the method of claim 2, wherein the number of rotating stack memory locations used for spilling and filling the computed values is equal to the number of simultaneous live values generated by the rotating register (e.g. FIGURE 7B-8B and related text and col. 31, lines 60-65 "... rotating registers that have been allocated ...").

Per claim 4, Srinivasan discloses a method comprising spilling and filling two or more computed values, held in a rotating register (col. 17, lines 21-25 "... the value stored in a memory location, the address ..."), that are live across multiple stages in a software-pipelined

loop using two or more corresponding rotating stack memory locations (e.g. FIGURE 5, element 532 and 530 and related text).

Per claim 5, Srinivasan discloses the method of claim 4, wherein the computed values are spilled and filled using two or more corresponding rotating stack memory locations (e.g. FIGURE 6, elements 620, 622 and related text).

Per claim 6, Srinivasan discloses the method of claim 4, wherein the computed values are Floating Point values (col. 17, lines 1-5 "... floating point ...").

Per claim 7, Srinivasan discloses a method comprising: checking for availability of rotating registers to hold computed values that are live across multiple stages in a software-pipelined loop (e.g. FIGURE 6, element 530 "Rotating Register Allocator"); and

spilling and filling the computed values held in rotating registers in a software-pipelined loop using rotating stack memory locations for rotating registers (col. 2, lines 30-40 "... fill pipeline ..."), when there are no rotating registers available to hold the computed values (col. 5, lines 5-12 "... none of the rotating registers ...").

Per claim 8, Srinivasan discloses the method of claim 7, wherein the computed values are Floating Point (FP) values (col. 17, lines 1-5 "... floating point ...").

Per claim 9, Srinivasan discloses the method of claim 7, wherein the rotating registers are FP rotating registers (col. 17, lines 1-5 "... floating point ...").

Per claim 10, Srinivasan discloses a method comprising: checking for availability of FP rotating registers to hold FP computed values that are live across multiple stages in a software-pipelined loop (e.g. FIGURE 6, element 530 "Rotating Register Allocator"); and

spilling and filling the computed values using rotating integer registers for holding addresses of stack memory locations when there are no FP rotating registers available to hold the computed value (col. 2, lines 30-40 "... fill pipeline ...").

Per claim 11, Srinivasan discloses the method of claim 10, wherein spilling and filling the computed value using the rotating integer registers comprises:

checking for availability of N+1 rotating integer registers, wherein N is number of stages a computed value that needs to be spilled is live in the software-pipelined loop (e.g. FIGURE 6, element 530 "Rotating Register Allocator"); and

spilling and filling the computed value in stack memory locations whose addresses are held in corresponding N+1 rotating integer registers, when the N+1 rotating integer registers are available (col. 5, lines 5-12 "... none of the rotating registers ...").

Per claim 12, Srinivasan discloses the method of claim 11, wherein spilling and filling the computed value comprises:

storing the computed value in the stack memory locations whose addresses are held in corresponding N+1 rotating integer registers (col. 19, lines 34-45 "... variable is stored ... register is spilled ..."); and

loading from the stack memory locations whose addresses are held in corresponding N+1 rotating integer registers based on number of stages between when the loading occurs from the storing of the corresponding computed value (col. 22, lines 15-23 "... loading values from ...").

Per claim 13, Srinivasan discloses the method of claim 10, wherein target registers for filling could be any available FP registers (col. 17, lines 1-5 "... floating point ...").

Per claim 14, Srinivasan discloses a method comprising using post-incremented memory operations for spilling and filling of live computed values, held in a FP rotating register (col. 17, lines 1-5 "... floating point ..."), that are live across multiple stages in a software-pipelined loop, using non-rotating registers, when there are no rotating integer registers available to hold rotating stack memory locations (e.g. FIGURE 6 and related text).

Per claim 15, Srinivasan discloses the method of claim 14, wherein using the non-rotating registers comprises: using the non-rotating integer registers (col. 28, lines 50-55 "... static registers ...").

Per claim 16, Srinivasan discloses the method of claim 14, further comprising:

checking for availability of N+1 non-rotating integer registers available for spilling and filling, wherein N is a number of stages a computed value that needs to be spilled is live in the software-pipelined loop (col. 16, lines 60-65 "... register usage is being determined ..."); and

spilling and filling the computed values in stack memory locations whose addresses are held in corresponding N+1 non-rotating integer registers, when the N+1 non-rotating registers are available (e.g. FIGURE 9C and related text).

Per claim 17, Srinivasan discloses the method of claim 16, wherein the rotating stack memory locations have to be contiguous and in descending order (col. 5, lines 65-67 and col. 6, lines 1-5 "... first static register is not available ...").

Per claim 18, Srinivasan discloses a method comprising spilling and filling of live computed values, held in a rotating register, that are live across multiple stages in a software-pipelined loop, using two non-rotating integer registers (e.g. FIGURE 5 and related text), when there are no FP rotating registers available and when there are no rotating integer registers available for holding rotating stack memory locations, and when there are not enough non-rotating integer registers available for holding rotating stack memory locations (col. 32, lines 40-45 "... holds the current address...").

Per claim 19, Srinivasan discloses the method of claim 18, wherein the two non-rotating registers do not have to be contiguous (e.g. FIGURE 5, elements 532, 530 and related text).

Per claim 20, Srinivasan discloses the method of claim 18, wherein the rotating stack memory locations have to be contiguous and in descending order (col. 5, lines 65-67 and col. 6, lines 1-5 "... first static register is not available ...").

Per claim 21, Srinivasan discloses a method comprising: checking for availability of rotating integer registers and non-rotating integer registers, to spill and fill computed values held in a FP rotating register, that are live across multiple stages in a software-pipelined loop;

spilling and filling the computed values, held in a FP rotating register (col. 17, lines 1-5 "... floating point ..."), using the rotating integer registers to hold the rotating stack memory locations, when there are no FP rotating registers available to hold the computed values (col. 2, lines 30-40 "... fill pipeline ...");

spilling and filling the computed values, held in the FP rotating register (col. 17, lines 1-5 "... floating point ..."), using the non-rotating registers to hold the rotating stack memory locations, when there are no FP rotating registers to hold the computed values and further when there are no rotating integer registers
available for holding rotating stack memory locations (col. 5, lines 5-12 "... none of the rotating registers ..."); and

spilling and filling the computed values held in the FP rotating register (col. 17, lines 1-5 "... floating point ..."), using two
non-rotating integer registers to hold the rotating stack memory locations, when there are no FP rotating registers to hold the computed values, where there are no rotating integer registers available, and further when there are only a few non-rotating integer registers available for holding rotating stack memory locations (col. 5, lines 65-67 and col. 6, lines 1-5 "... first static register is not available ...").

Per claim 22, Srinivasan discloses the method of claim 21, wherein spilling and filling the computed values using the rotating integer registers comprises:

checking for availability of N+1 rotating integer registers, wherein N is number of stages a computed value that needs to be spilled is live in the software-pipelined loop (e.g. FIGURE 6, element 530 "Rotating Register Allocator"); and

spilling and filling the computed values in stack memory locations whose addresses are held in corresponding N+1 rotating integer registers, when the N+1 rotating integer registers are available (col. 5, lines 5-12 "... none of the rotating registers ...").

Per claim 23, Srinivasan discloses the method of claim 21, wherein spilling and filling the computed values using non-rotating integer registers comprises:

checking for availability of N+1 non-rotating integer registers available for spilling and filling, wherein N is a number of stages a computed value that needs to be spilled is live in the software-pipelined loop (col. 16, lines 60-65 "... register usage is being determined ..."); and

spilling and filling the computed values in stack memory locations whose addresses are held in corresponding N+1 non-rotating integer registers, when the N+1 non-rotating registers are available (e.g. FIGURE 9C and related text).

Per claim 24, Srinivasan discloses the method of claim 21, wherein the two non-rotating registers do not have to be contiguous (col. 5, lines 65-67 and col. 6, lines 1-5 "... first static register is not available ...").

Per claim 25, Srinivasan discloses the method of claim 21, wherein the rotating stack memory locations have to be contiguous and in descending order (e.g. FIGURE 6 and related text).

Per claim 26, this is the article version of the claimed method discussed above (Claim 1), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Srinivasan.

Per claim 27, this is the article version of the claimed method discussed above (Claim 21), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Srinivasan.

Per claim 28, this is the article version of the claimed method discussed above (Claim 22), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Srinivasan.

Per claim 29, this is the article version of the claimed method discussed above (Claim 23), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Srinivasan.

Per claim 30, this is the system version of the claimed method discussed above (Claim 21), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Srinivasan.

Per claim 31, this is the system version of the claimed method discussed above (Claim 22), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Srinivasan.

Per claim 32, this is the system version of the claimed method discussed above (Claim 23), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Srinivasan.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isaac T. Tecklu whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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